

ATLAS-IN2P3 contribution to the upgrade of the Inner Tracker

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on behalf of the IN2P3 ATLAS groups

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Layout

The Phase-II upgrade and the ITk

Recent contributions of French groups and implications for the ITk construction

- Sensors

- Planar pixel sensors, active edges, thin sensors
 - HVCMOS option

- Electronics

- Pixel readout electronics: RD53

Module construction proposal in the Paris cluster

- Mechanics and services

- Layout studies / simulations

- Thermo-mechanical developments

- Flexes

Stave assembly and test proposal in the CPPM / LPSC / LAPP cluster

Schedule for the ITk

A word on FastTrack and FTK++

High luminosity consequences for the ATLAS tracker

After Run 2-3 the present detector would not be adequate any more

Instantaneous conditions

- pileup and high event rate
- increased occupancy

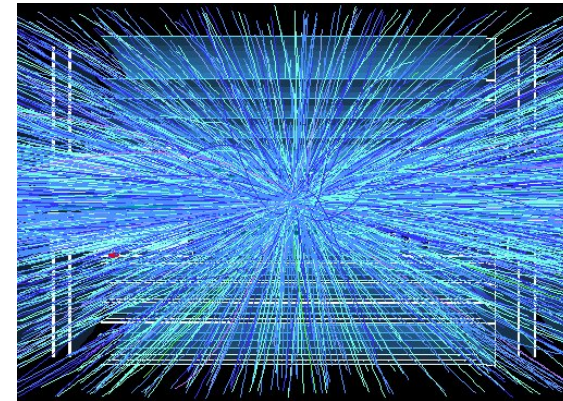
- higher granularity sensor
- SEU-robust, faster readout

Integrated effects

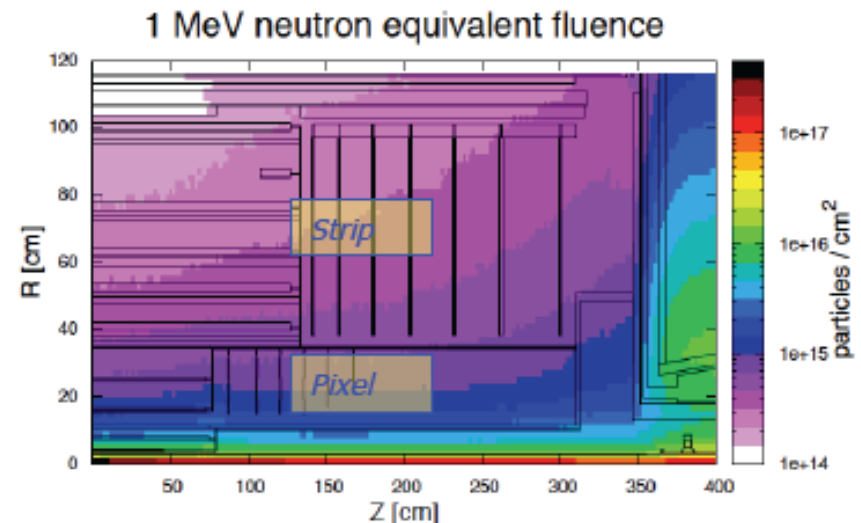
(radiation dose)

- leakage current
- change in operation voltage
- reduced charge collection

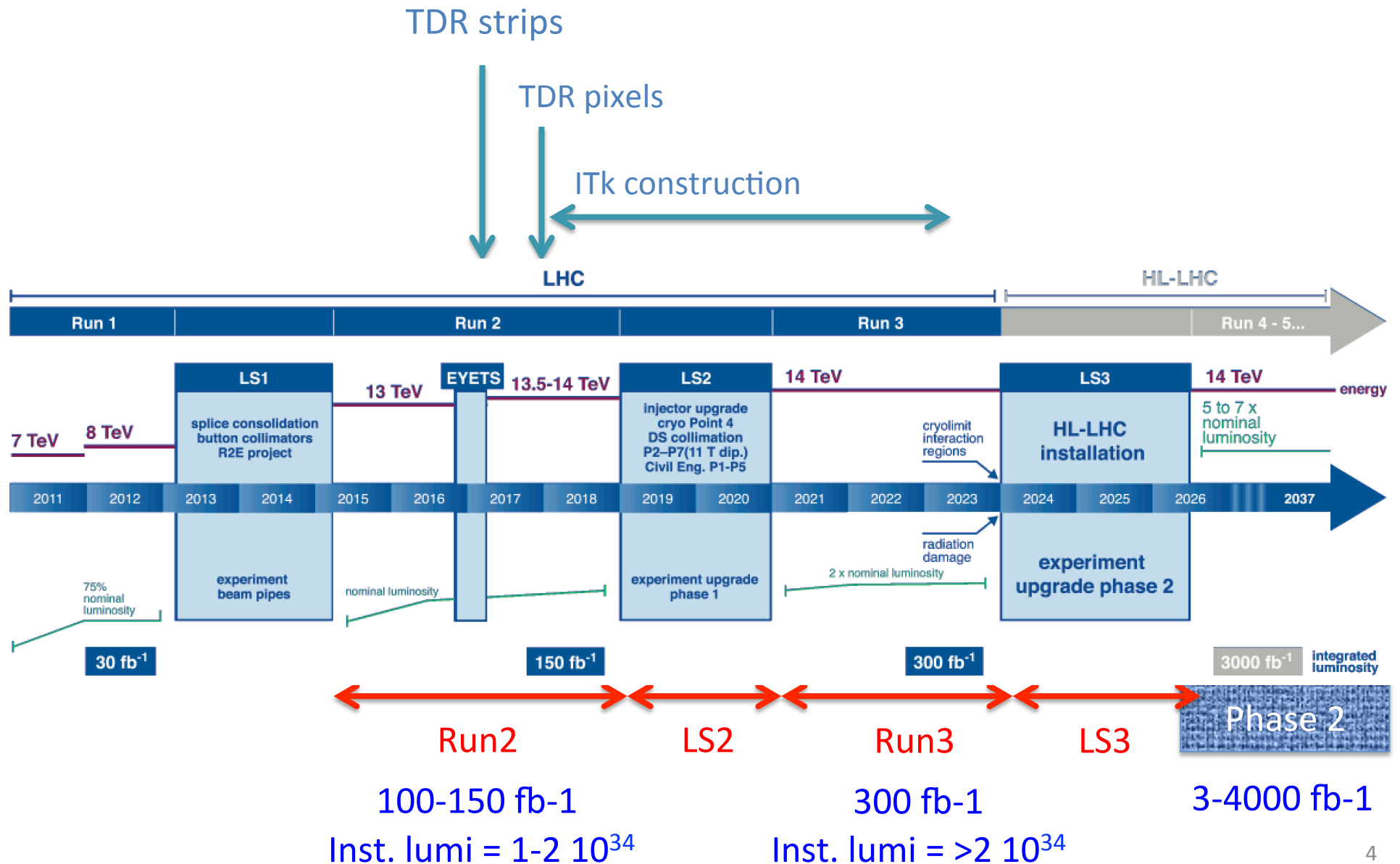
- rad-hard components
- thin sensors (partial depletion)



- Peak luminosity: $5-7 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$ $\rightarrow \sim \text{x}5-7$
- Average pile-up: up to $\langle \mu \rangle \sim 200$ $\rightarrow \sim \text{x}8$
- Integrated luminosity: 3000 fb^{-1} $\rightarrow \sim \text{x}10$
- Requested radiation hardness: $2 \times 10^{16} \text{ n}_{\text{eq}}/\text{cm}^2 \rightarrow \text{x}20$



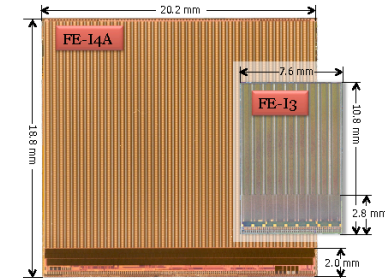
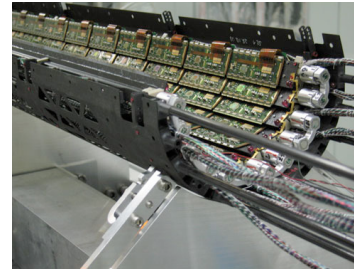
The ATLAS ITk roadmap to the LHC upgrade



French groups have historically contributed to the ATLAS pixels and to IBL

CPPM has participated to the design and construction of the original ATLAS pixel detector

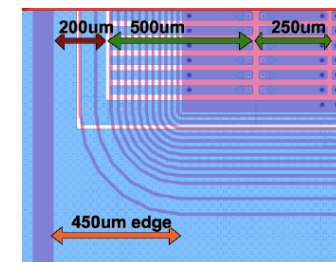
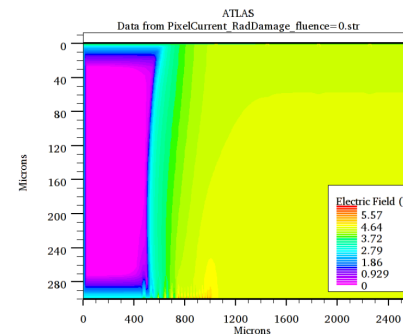
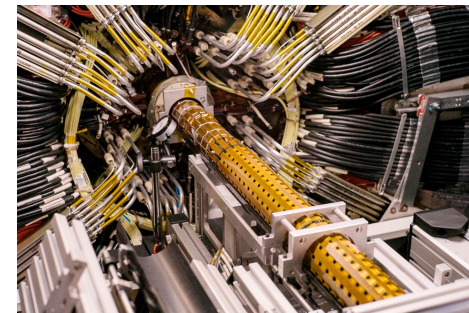
- mechanical structure of staves,
- readout electronics (FE-13)
- strong contribution in stave assembly



LAL, LAPP, LPNHE, LPSC joined CPPM for the design and construction of the 4th layer (IBL)

Among other contributions:

- stave conception (CPPM)
- design of sensors, increased efficiency at the border (LAL, LPNHE)
- readout electronics FE-14 (CPPM)
- electrical services (LAPP, LPSC)
- cooling services and interconnections (LAPP, LAL, LPNHE)
- design of the IBL insertion tooling (LPSC)



How will the ITk look like?

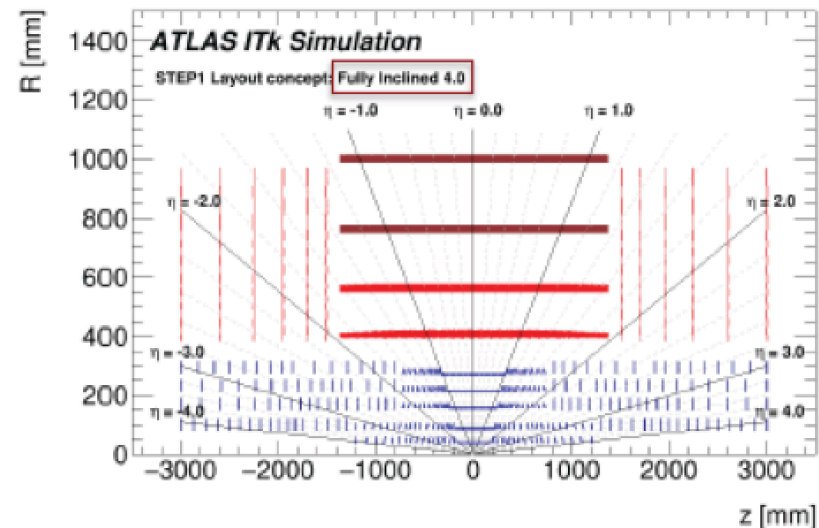
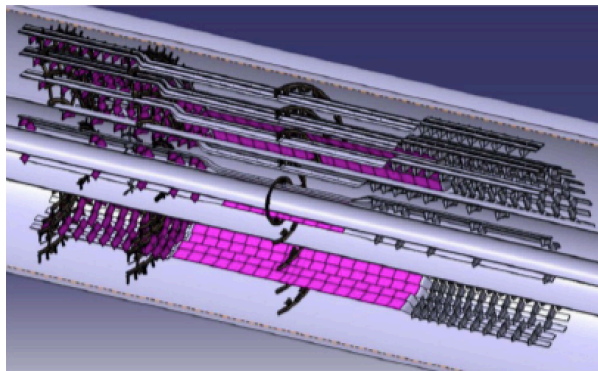
Some general constraint clear since the beginning

- ✓ Pixel volume up to 345 mm radius; then strips to the edge of the solenoid
- ✓ 5 pixel barrel layers + 3 or 4 rings, total surface $\sim 14 \text{ m}^2$
- ✓ 4 strip barrel layers + 2x6 endcap discs
- ✓ η coverage up to 4.0, at least 9 space points
- ✓ small pixels: $50 \times 50 \text{ }\mu\text{m}$ or $100 \times 25 \text{ }\mu\text{m}$
- ✓ pixel innermost detector replaceable (it is inside the Inner Support Tube)

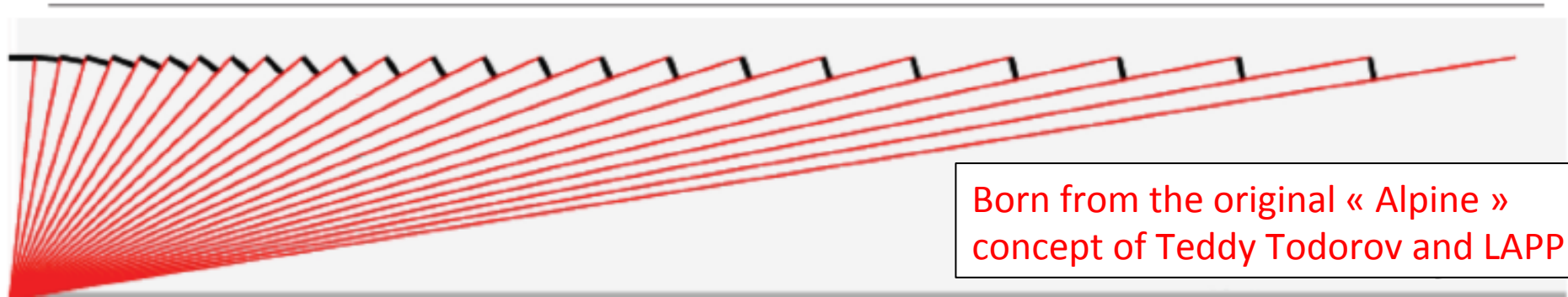
Layer	Radius present pixels (mm)	Radius ITk (mm)
0	33.5	39
1	50.5	75
2	88.5	155
3	122.5	213
4	-	271

A task force called LTF (Layout Task Force) has been in charge to give a recommendation among different options for the general layout of the system (2016 to beginning 2017)

An “Inclined layout” option preferred to a classical barrel layout extended to $\eta = 4$

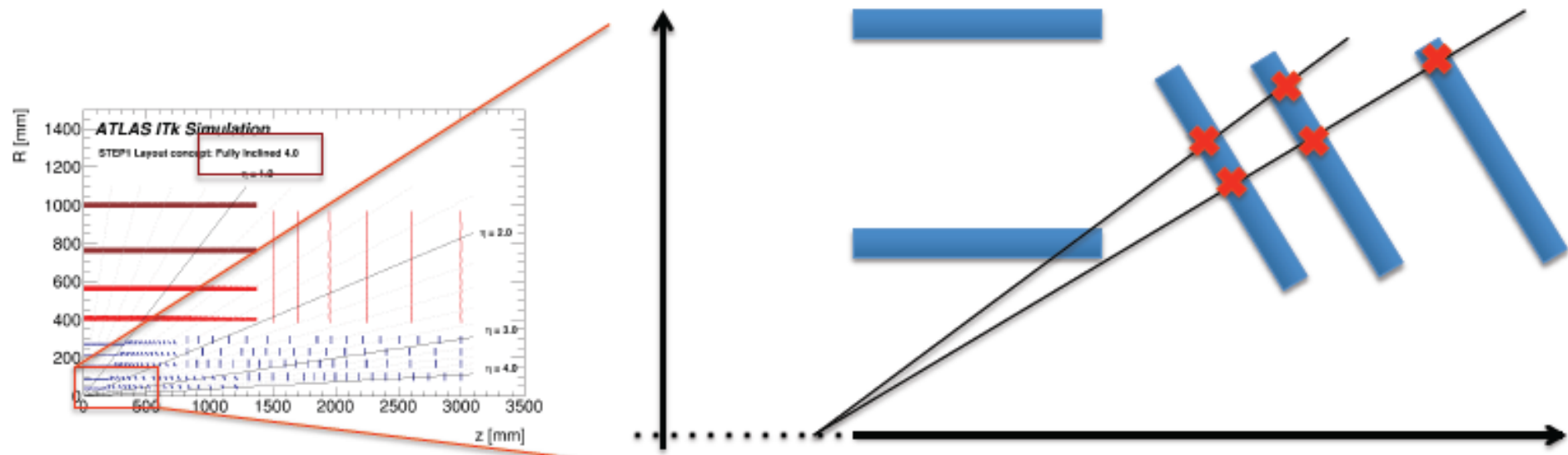


“Inclined” concept



✓ From ideas to layout:

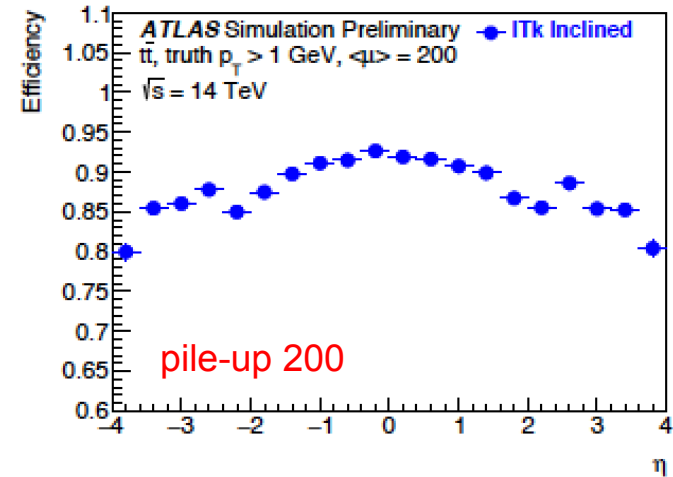
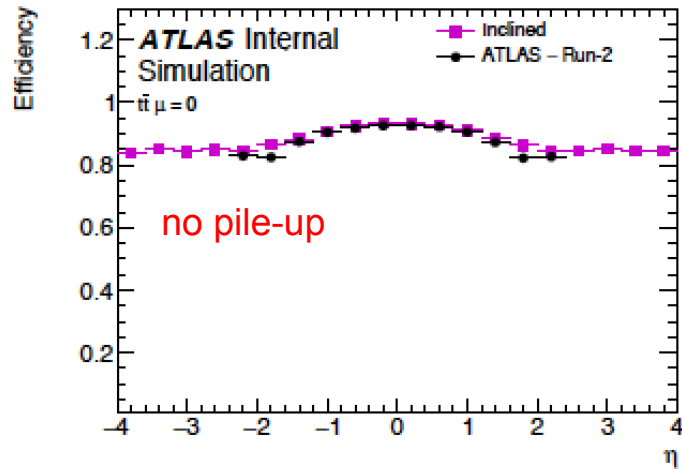
- Sensors are designed to be “perpendicular” to the particles trajectories, reducing the material seen by the particles.
- “Tracklets” are reconstructed increasing the number of hits per layer.



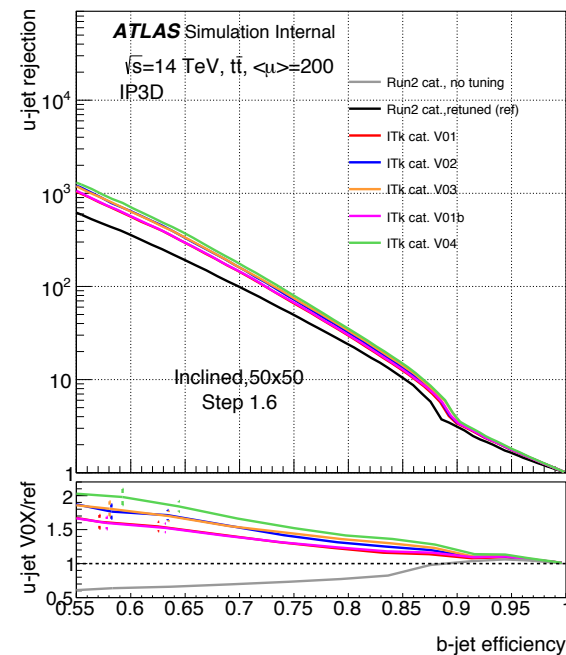
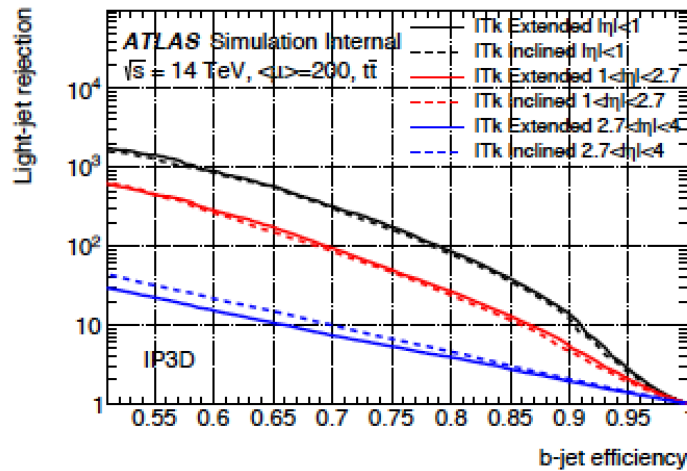
In addition, reduced silicon surface 7

Track reconstruction efficiency and b-tag performance

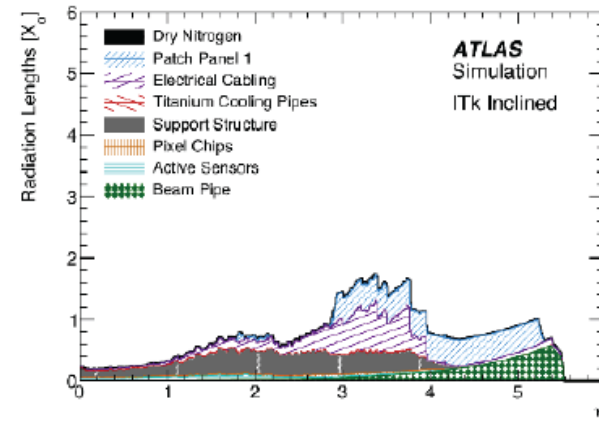
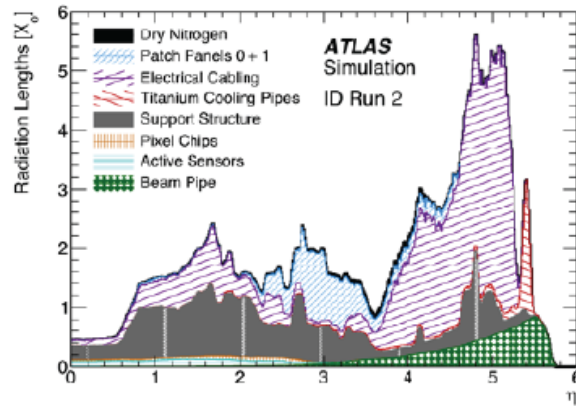
Comparison also with the present system



IP3D



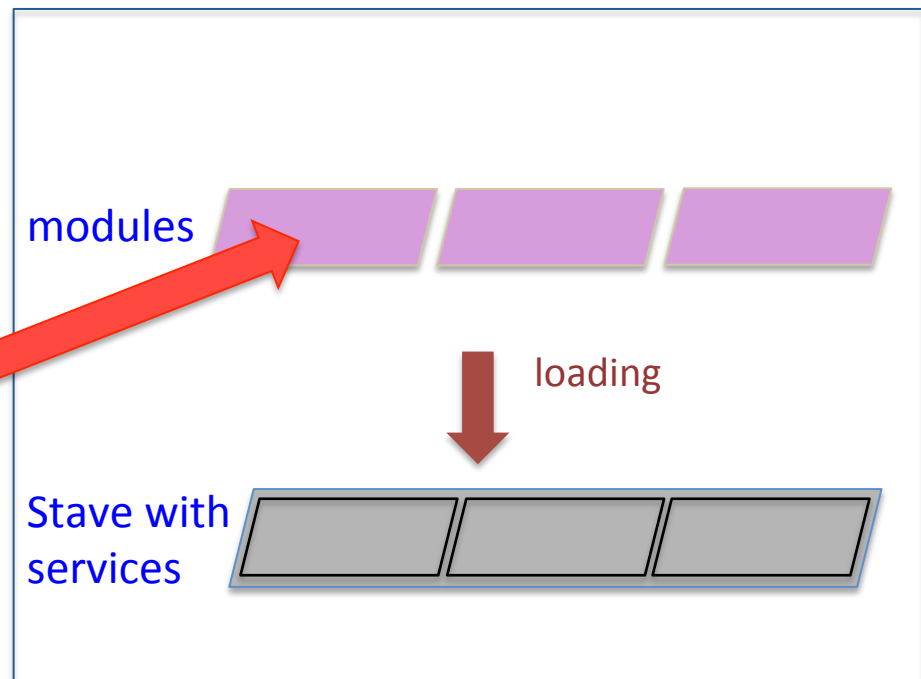
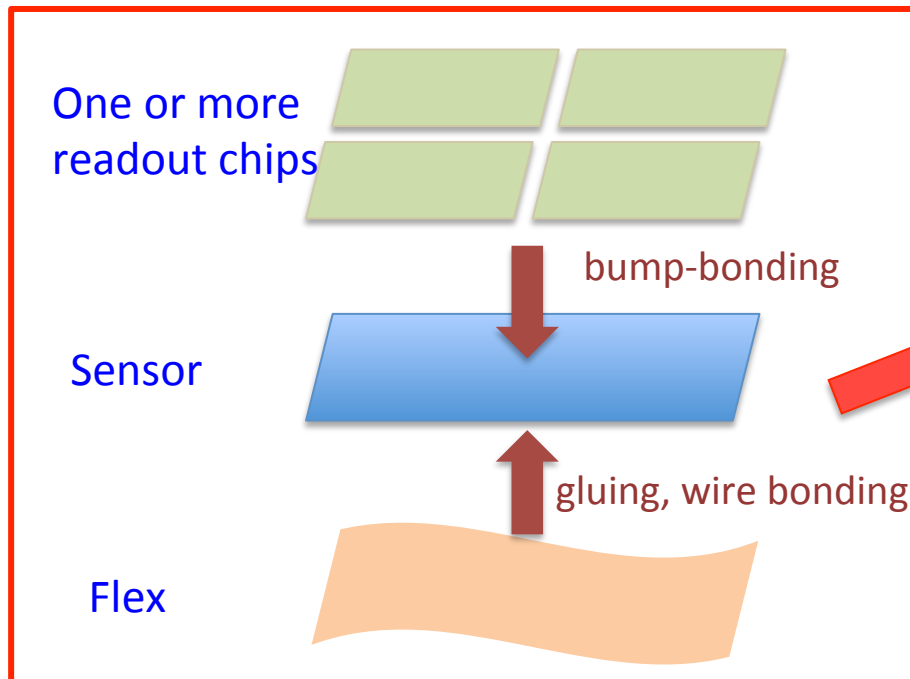
Important reduction in material budget



A bit of jargon to understand the ATLAS pixels

“Module”

“Stave loading”



Sensors and electronics are monolithic for HV-CMOS

A possible layout

+ contingency / spares !

France potentially interested in outer barrel, with three more big funding agencies

Ballpark of 1000-2000 modules to build

	# staves/rings	# modules	total staves/rings	total modules
Layer 0	16	704	36	1424
Layer 1	20	720		
Ring 0	8	128	128	4600
Ring 1	14	308		
Layer 2	30	960		
Layer 3	42	1512		
Layer 4	56	2128		
Ring 2	20	680		
Ring 3	16	768		
Ring 4	18	1044		

Endcap 1

(planar)

Outer Barrel

L4 (planar, HV-CMOS?)

L2 / L3 (planar)

Endcap 2

(planar)

Inner Section

L0 / L1 (3D/planar)

Contribution of French groups

The ATLAS French groups are strongly participating to the ITk and have an important role in the construction

- Important French contribution to the layout and performance studies
- French laboratories had a leading role in the development of basically all the detector components
- Solid plan to participate to the construction of modules and to the loading of staves and detector integration
- Important participation in the ITk pixel TDR (French editors of sections) and in working groups / operations groups

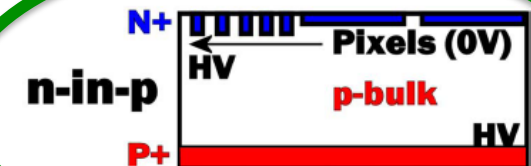
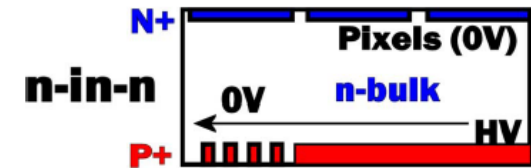
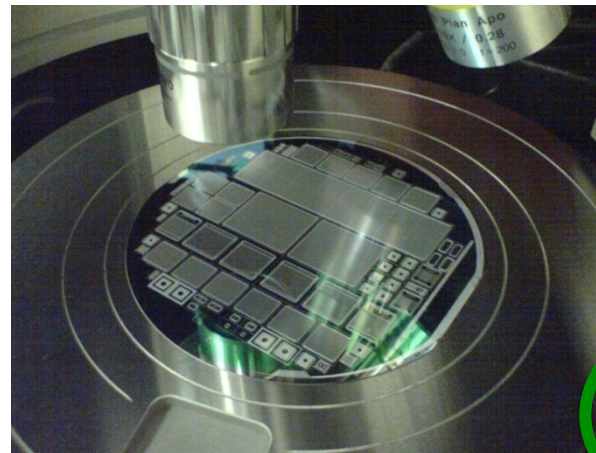
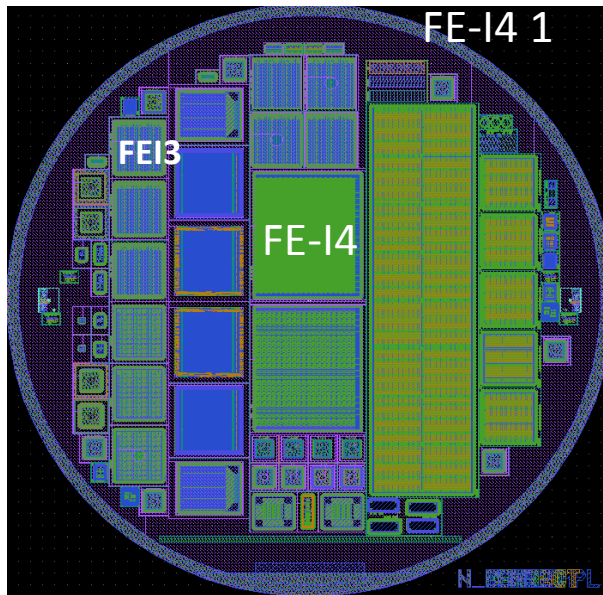
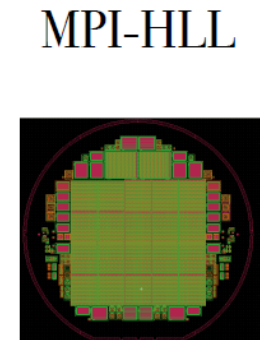
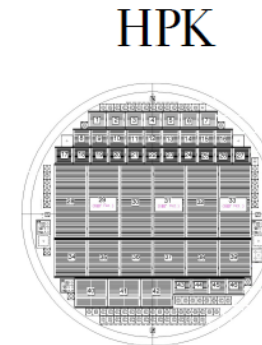
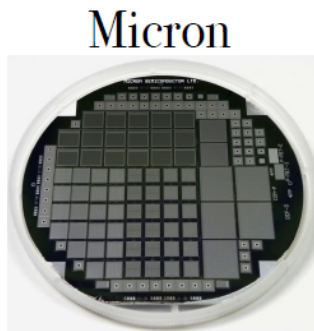
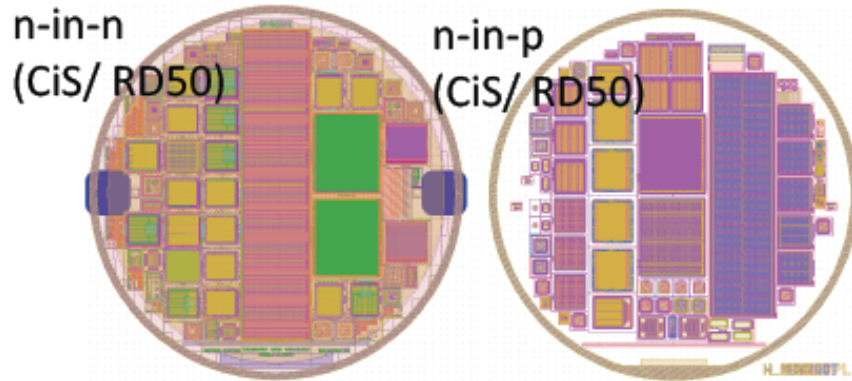


Sensors



Planar Pixel Sensors

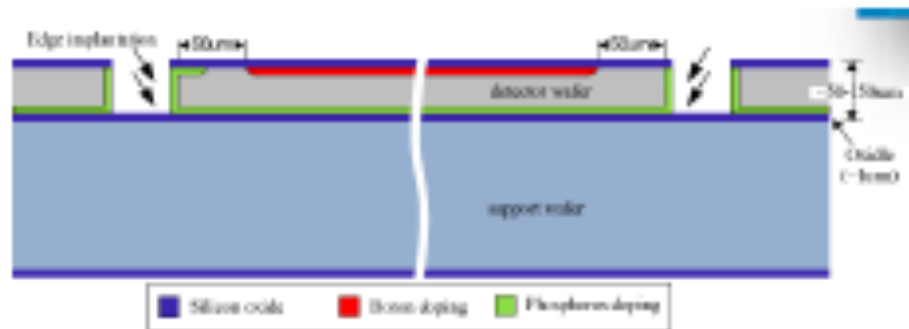
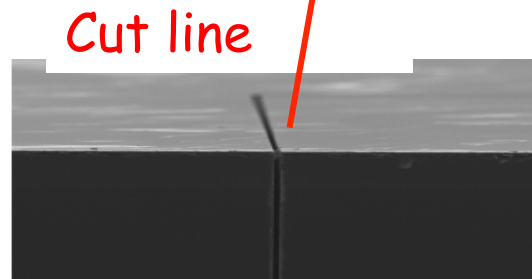
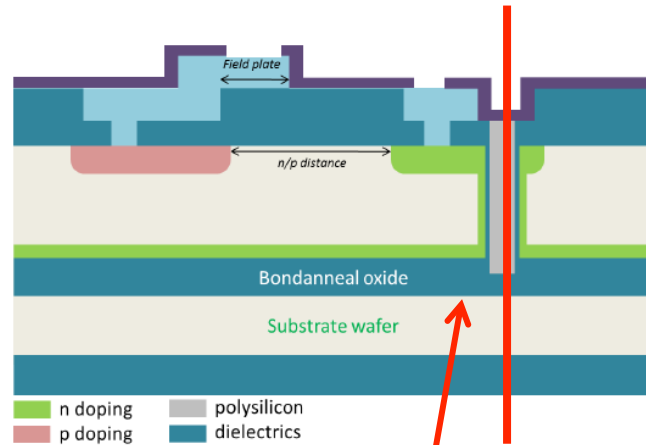
In the years, many R&D productions for IBL and SLHC
(very active part of IBL and now of ITk)



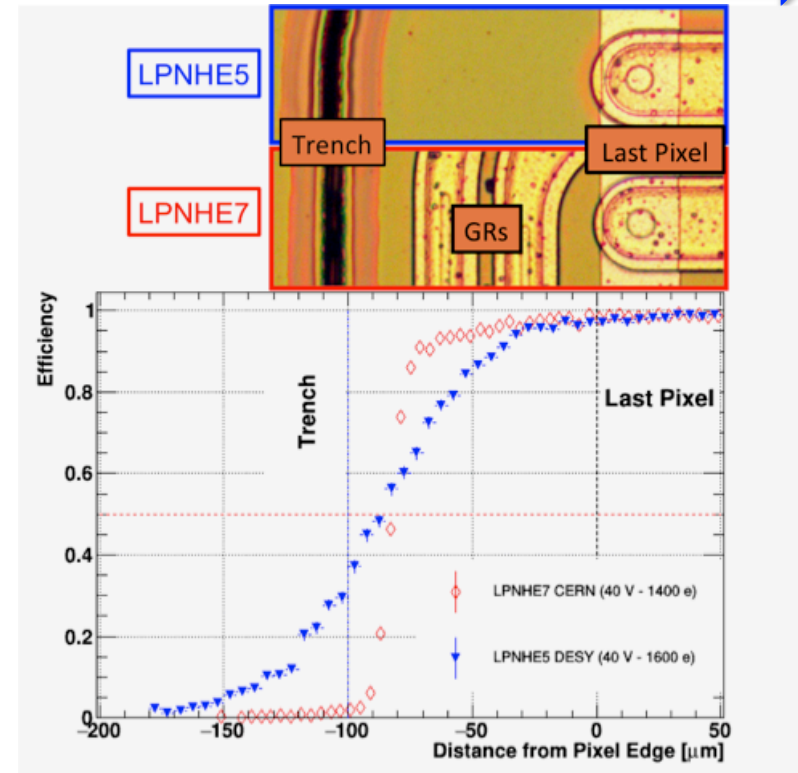
See: ATL-UPGRADE-PUB-2010-001; Nucl.Instrum.Meth. A730 (2013) 215

Cheaper and more
rad-hard than n-in-n;

Active-edge and thin sensors



JINST 12 P05006 (2017)

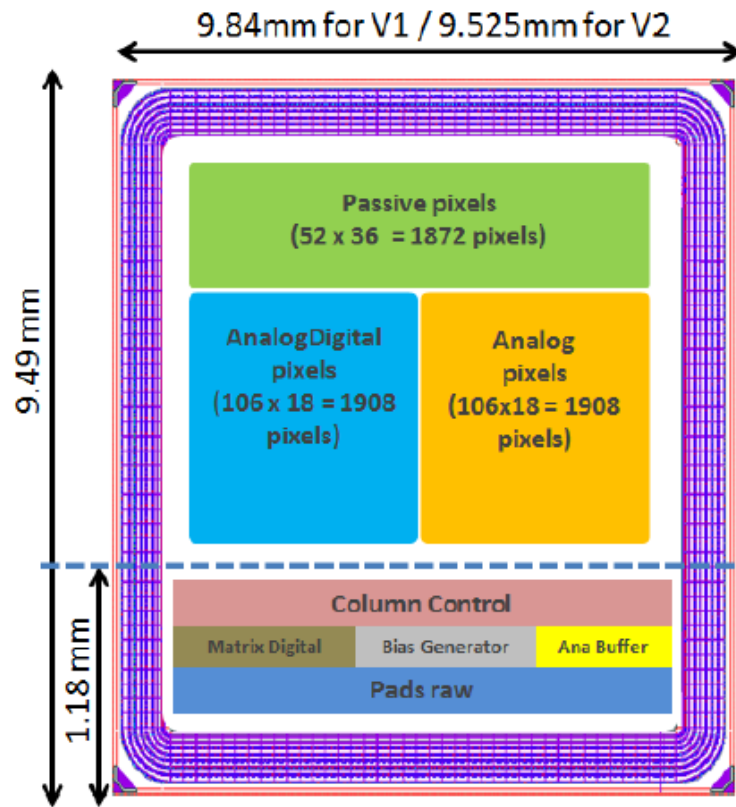


Capacity to maintain good efficiency beyond pixel region (active edge concept)

FBK (Italy), Advacam (Finland) productions: 50 - 100 - 130 μm

FBK: Common ATLAS-CMS

Recent developments HV/HR-CMOS



LFoundry 150nm

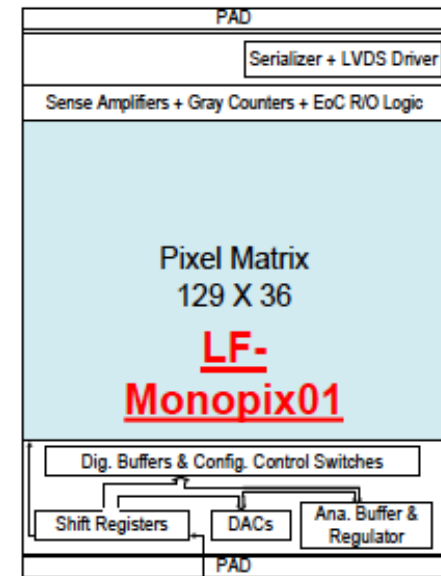
CPIX

Technology takes advantage of commercial CMOS process.

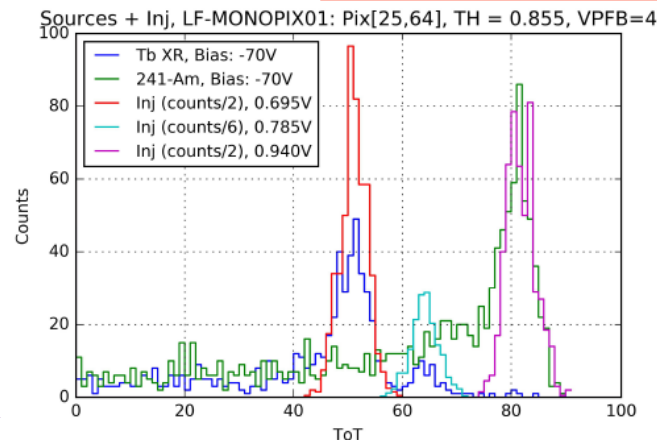
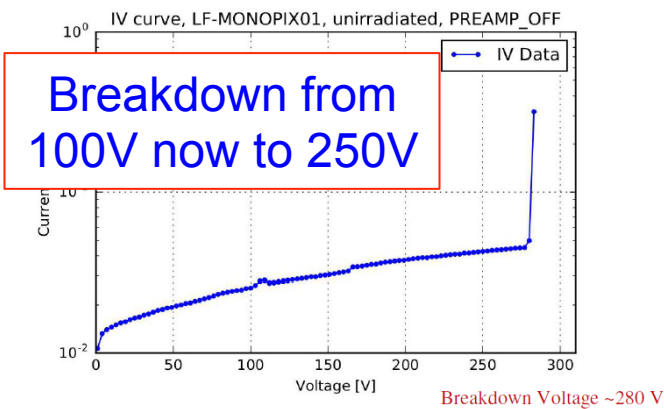
- Reduce costs, module complexity, increase turn around time.
- Reduce cluster size at high pseudo-rapidity.

Could be an option in the outer layers → **Targets the pixel 5th layer in TDR(monolithic flavor)**

measurements with injected charge and 241-Am (green)



Monolithic: Monopix01





Electronics



RD53

Collaboration for a common ATLAS-CMS pixel readout chip in 65nm; This chip will also be used to test sensors for the development and the preproduction

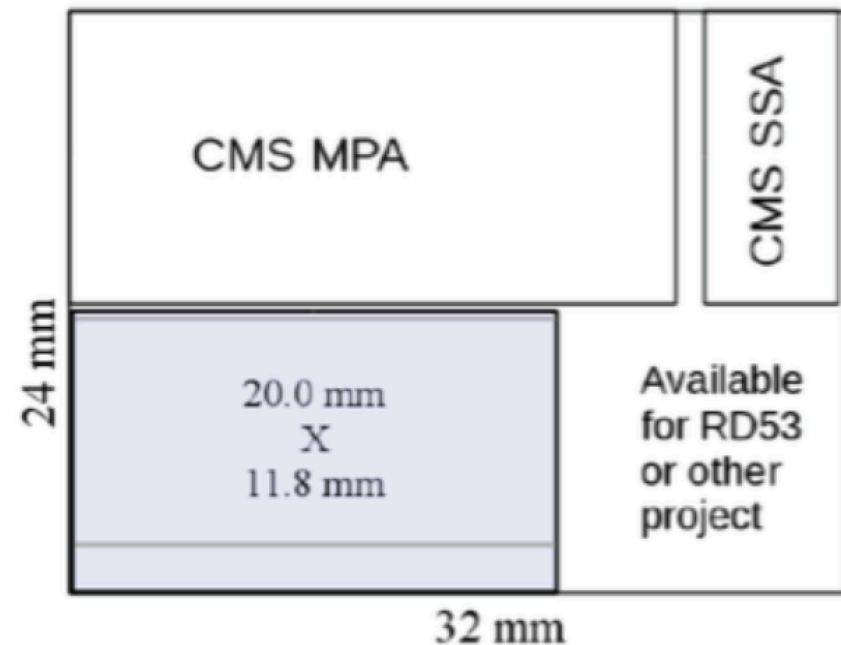
- ✓ First demonstrator 20 x 11.8 mm
- ✓ 400 x 192 pixels of 50 x 50 μm
(final chip will be $\sim 400 \times 384$)
- ✓ 65 nm technology
including radiation tolerance >500 Mrad
- ✓ Trigger rate: 1 MHz
- ✓ Low in-time threshold: 1200 e^-
- ✓ Test of serial powering

Specs document:

CERN-RD53-PUB-15-001

<http://cds.cern.ch/record/2113263>

RD53a



expected delivery:
October 2017

RD53

Specific contributions:

CPPM

- Radiation characterization and modeling
- Analog column bottom (ACB) organization
- In-pixel single event upset SEU-hard latch
- IP blocks

LPNHE

- Contribution to Digital Design and I/O groups
- Transmission protocol Aurora 64b66b (VHDL code)

LAL

- Oscillator to characterize the performance after radiation

Being part of the collaboration will allow to be among the first institutions to have access to the RD53a chips for characterization and use with sensors

Now very important to be ready for the test of delivered chips and to connect them to our sensors, in view of the TDR

Start developing test benches / infrastructure

Module construction

Planar sensor testing and module construction

Above-described experience in sensor production and test and electronics design have pushed the LPNHE and LAL group to propose a cluster of module construction in the Paris region (in collaboration with the IRFU ATLAS group)

Already existing infrastructure



Wafer probing capabilities
in all the sites

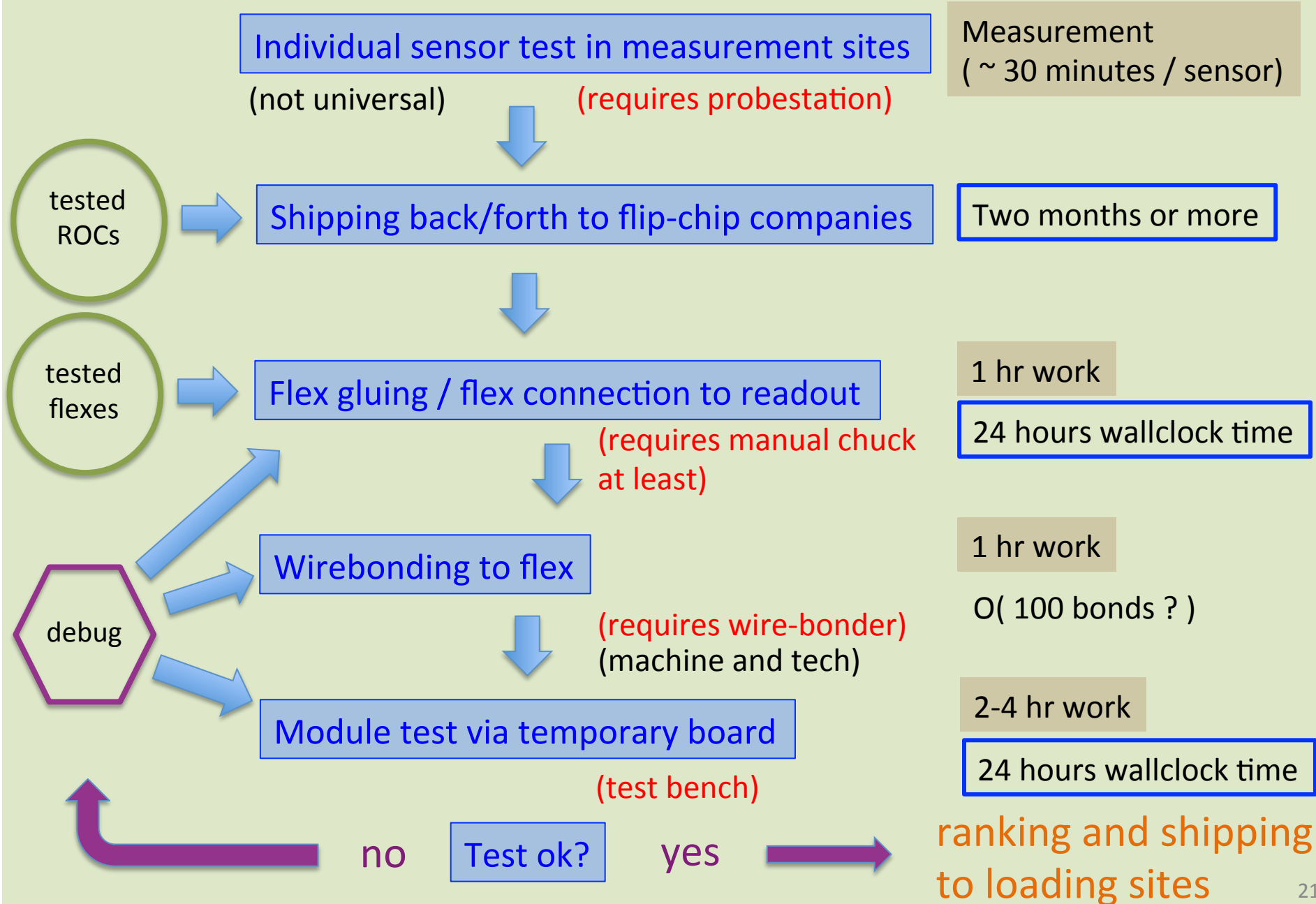


Bonding capability



Preliminary evaluation suggests capability of the site to produce between 1000 and 2000 quad modules / 2 years (number will be negotiated with ATLAS)

Flowchart for module assembly / Test (simplified sketch)



Some considerations on module construction

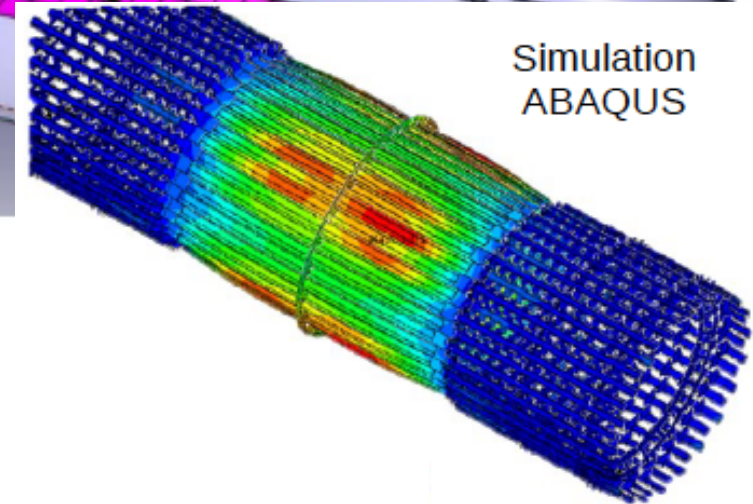
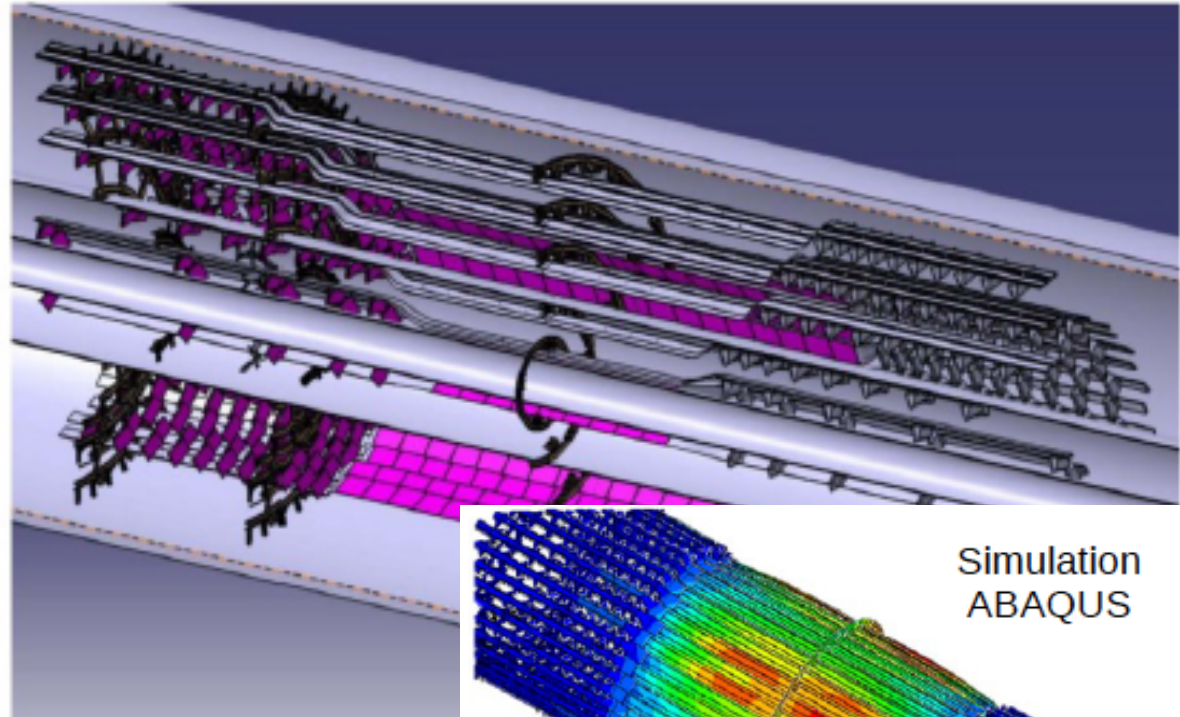
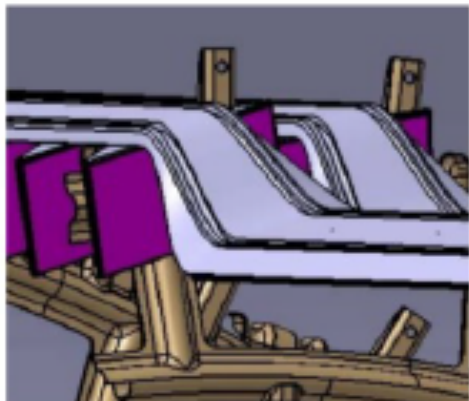
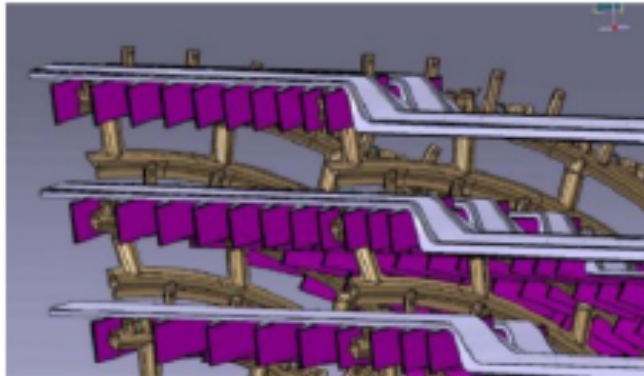
- The quantity of 1000-2000 modules in two years seems to be conservative but problems can always arise and we don't want to underestimate the time necessary to understand and solve them
- For normal operations, some step requires parallelism (for instance the test suite)
- Redundancy is critical both in terms of manpower and infrastructure

In the module construction operation, with the present resources, the sector in which some criticality might arise seems to be in the wirebonding part.

Redundancy should probably be enforced through the procurement of a second bonding machine

Mechanics and services

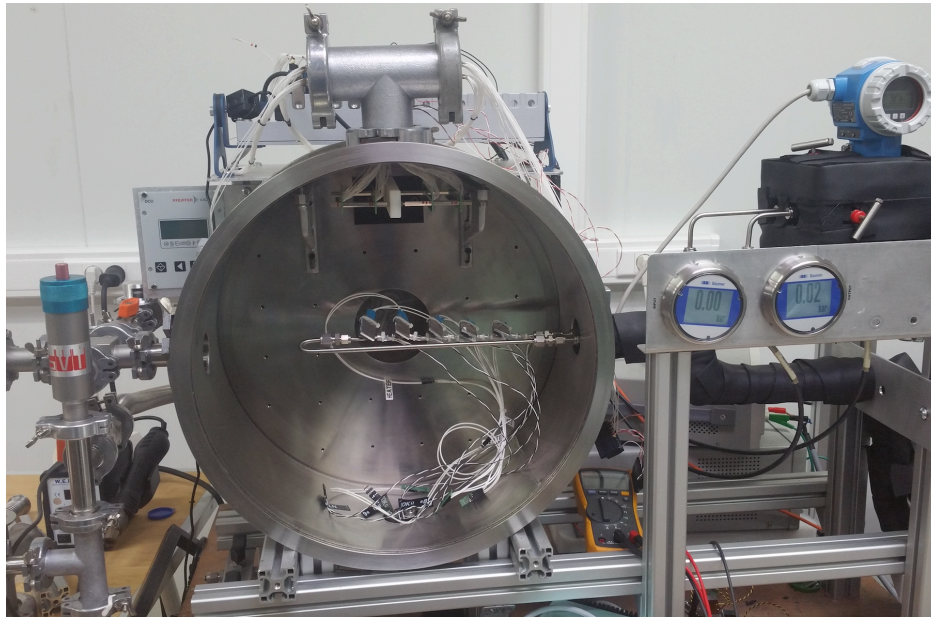
Big French contribution to the general layout and the mechanical conception



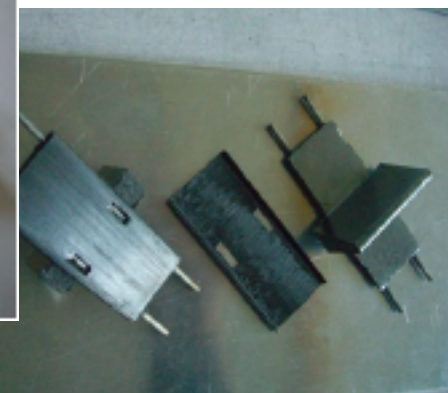
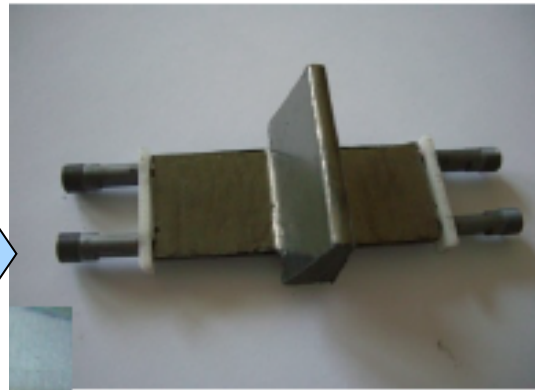
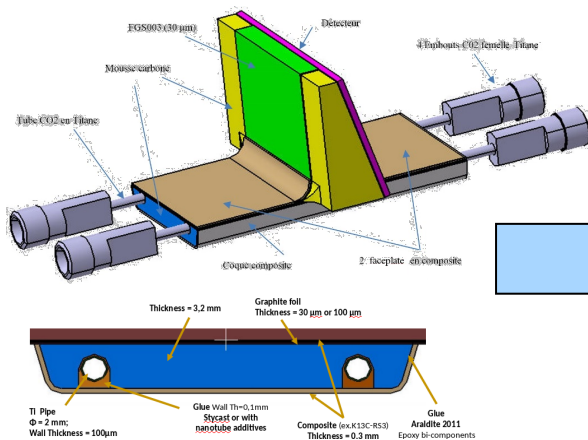
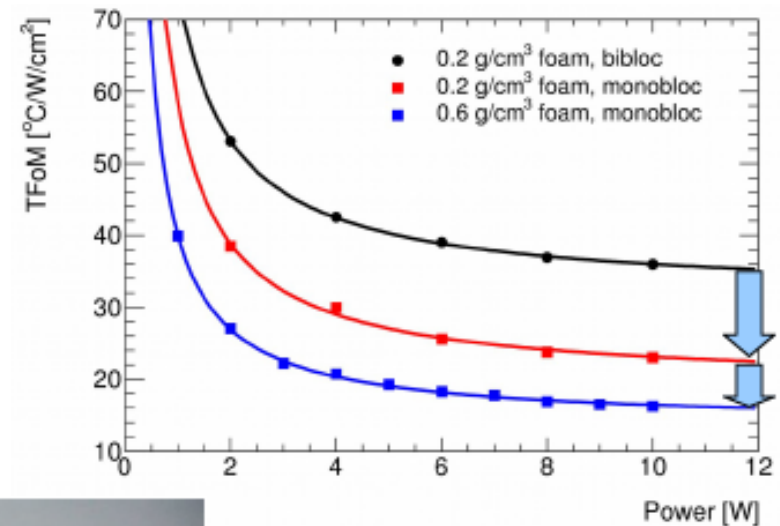
Static and modal studies of stave bending (optimization for global system)

Thermal characterization of components

Setup and measurements



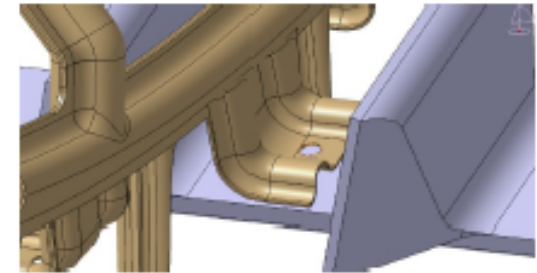
Able to show that the Alpine stove prototypes comply with the specifications



Prototype construction

Thermo-mechanical validations

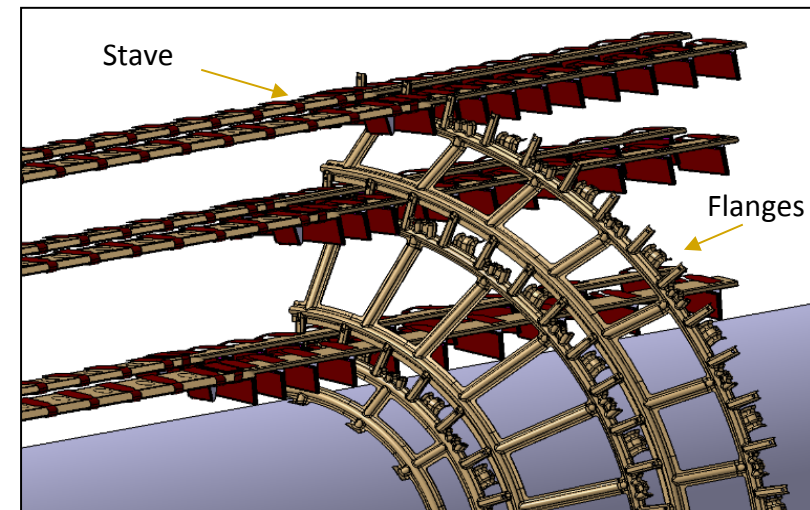
- ◆ Performance: stave/flanges links assumption
 - studies ongoing to check the influence on the detector behaviour
 - FEA + tests at LPSC



- ◆ In 2017: thermo-mechanical characterisation of components
 - laser bench to be developed



Laser Bench (dynamic+sag)



Configuration for mechanical simulations and tests

Development of stave flex



ALPINE

(Flex running below the carbon stave)



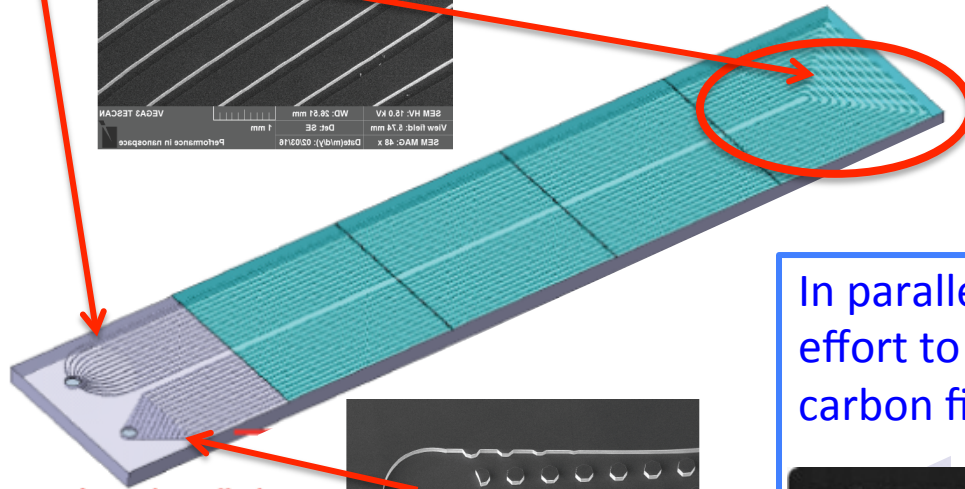
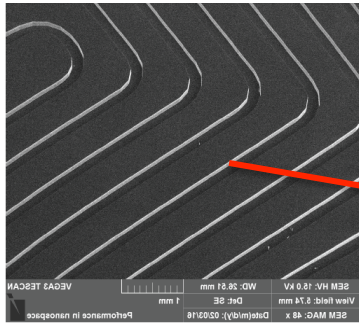
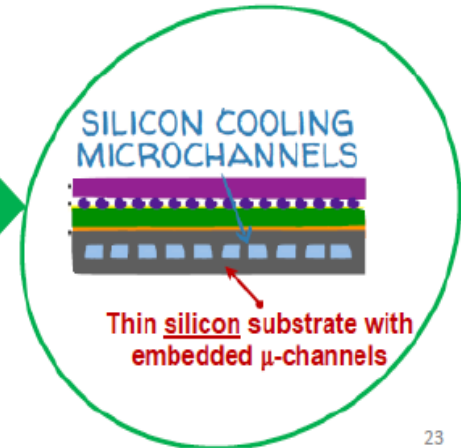
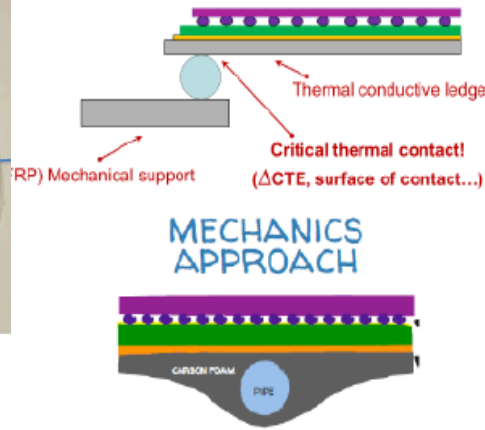
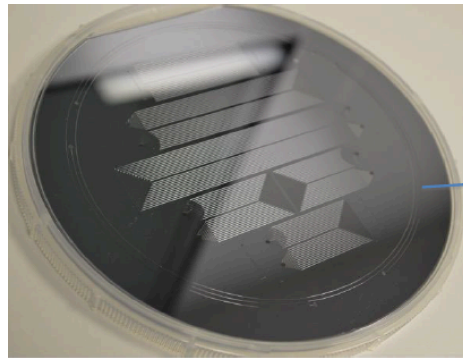
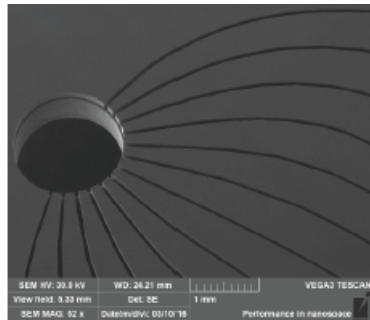
SLIM

(Flexes running along the sides of the longeron)

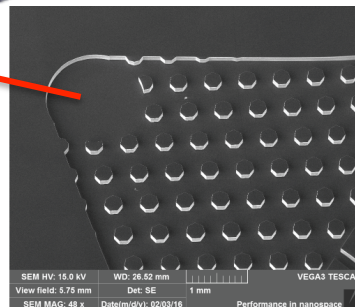


- Design and prototyping and test of stave flex
- Development of the installation procedure
- Interface with module flexes (connectivity, active logic)
- Well on track for industrial production

Option: micro-channels for cooling

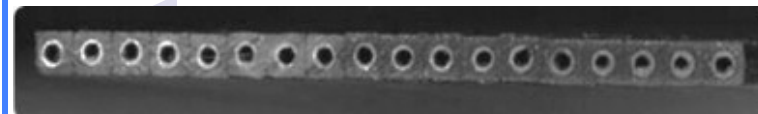


With FBK and IEF Orsay



Still a lot of work to do for the interconnections. It will not certainly be the baseline in the TDR but will represent a valid option in the mid-term replacement of ITk innermost pixel layers

In parallel, in the framework of AIDA-2020, effort to evaluate blocks of single tubes in carbon fiber, glued together.



F.Bosi et al.
Nucl.Instrum.Meth. A650 (2011) 213-217

Module loading on staves and tests

Staves construction and tests

- Significant experience of CPPM in the stave loading of the present ATLAS pixel system
- Important above-described experience of LAPP and LPSC in design and construction of services

Proposal to have a French module loading cluster, with construction activities in CPPM and LPSC and component design, production and test in LAPP

(Members of all the five IN2P3 ITk laboratories will finally participate to the tests and integration in the assembly sites and at CERN, to contribute to the test / rework of the components they developed)

Stave assembly

(CPPM, LPSC, and collaboration with LAPP)

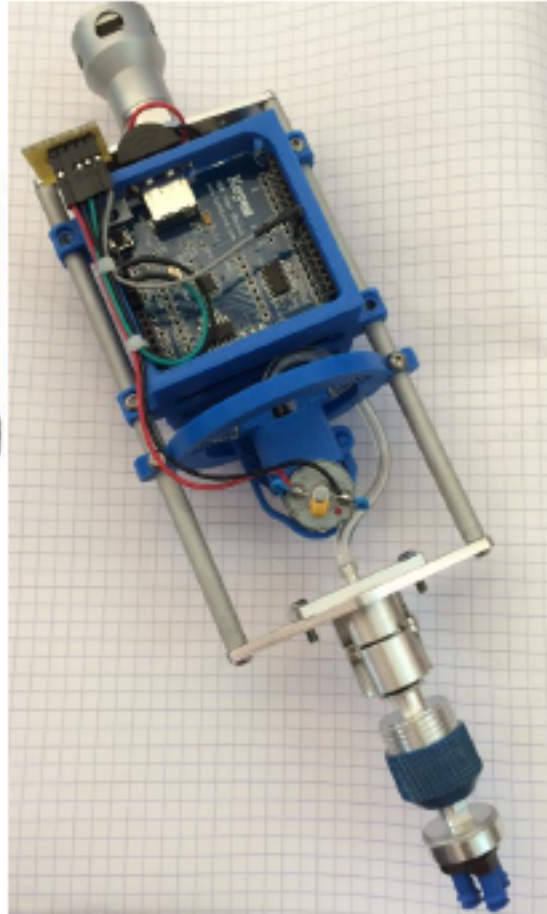
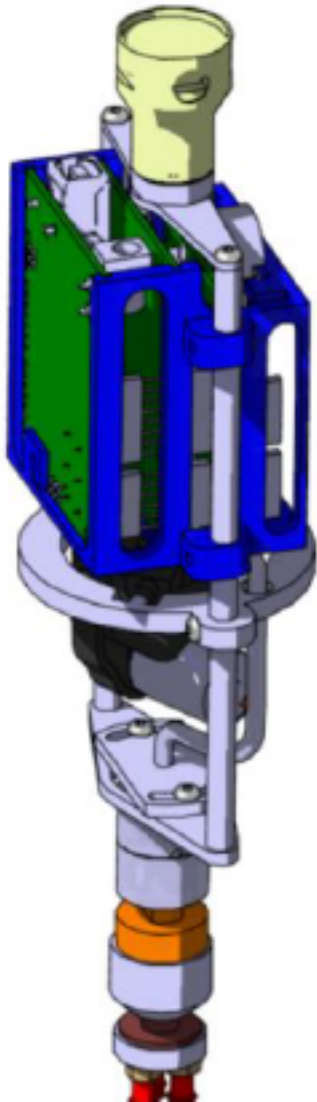


Mitutoyo machine adapted for element manipulation (solution adopted by other groups using the same machine)

Range: 900 x 1600 x 800 mm

Standardization of methods, procedures, software

Préhenseur horizontal: done



Different utilities developed to be installed on the Mitutoyo to perform the necessary operations



LPSC and LAPP could also take part of the preparation of the staves and the testing suite

Connectivity tests, burn-in, thermal cycles, thermal characterization

Some considerations on stave assembly

- A number of full staves between 35 and 50 in two years seems to be a reasonable proposal for the French cluster
- As in the case of module construction, redundancy is critical also for the operation of stave construction
This is both in terms of manpower and infrastructure

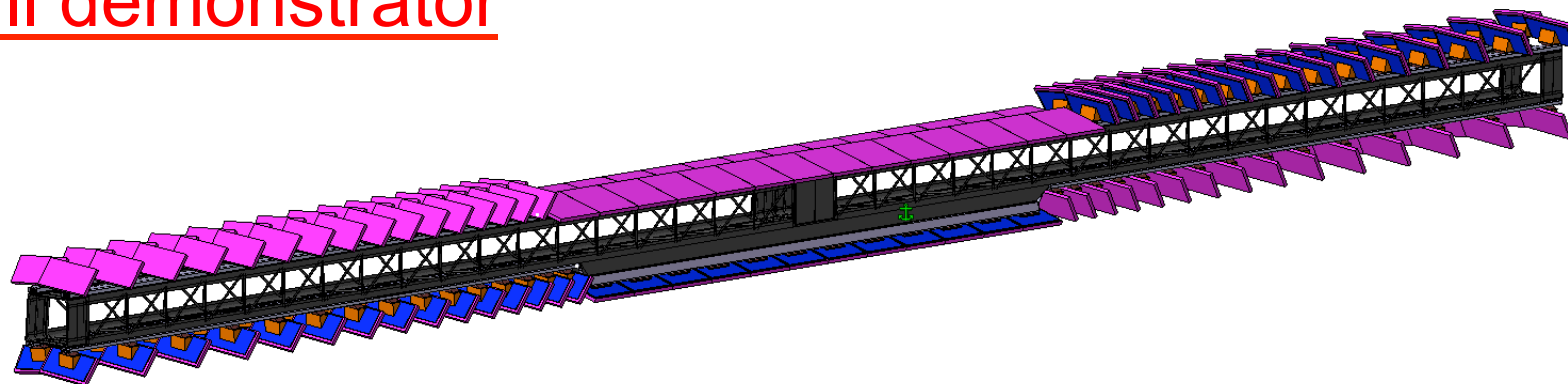
In this sense, the presence of just one Mitutoyo machine in the cluster could represent an issue for redundancy.

The procurement of a second machine identical to the one used in CPPM and located on the LPSC site will enforce protection against unexpected circumstances which could generate delays or even stop temporarily the stave production.

Implementing and testing the ITk construction sequence

The construction of the ITk Demonstrator

Ongoing ATLAS activity to produce a 4-staves full demonstrator



One stave fully active, the other three are thermal dummy staves to test the cooling solutions and their performance

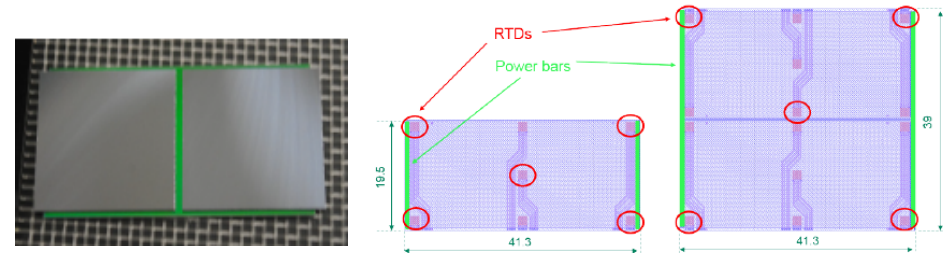
Program to evaluate and validate inclined concept

- Evaluate Thermal fluidic and electrical properties
- Validate prototypes, module construction and loading procedures
- Exercise integration and develop tooling
- Install and commission system setup (CO₂ cooling, power, interlocks)

Tight timescale driven by readiness for the pixel TDR (end 2017)

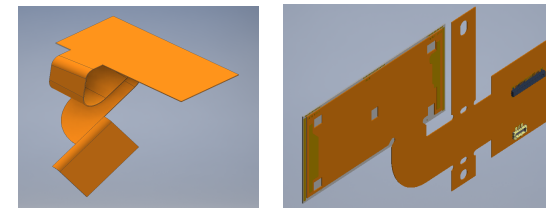
Sensors: LPNHE and LAL are involved in the production of both real (dual modules) and thermal modules for the demonstrator.

This will be used as a proof of principle of the module construction capability.



Thermal measurements: LPSC will do thermal characterization of produced modules, as well as prototyping of local supports. CPPM will measure mechanical stability and deformation for thermal effects

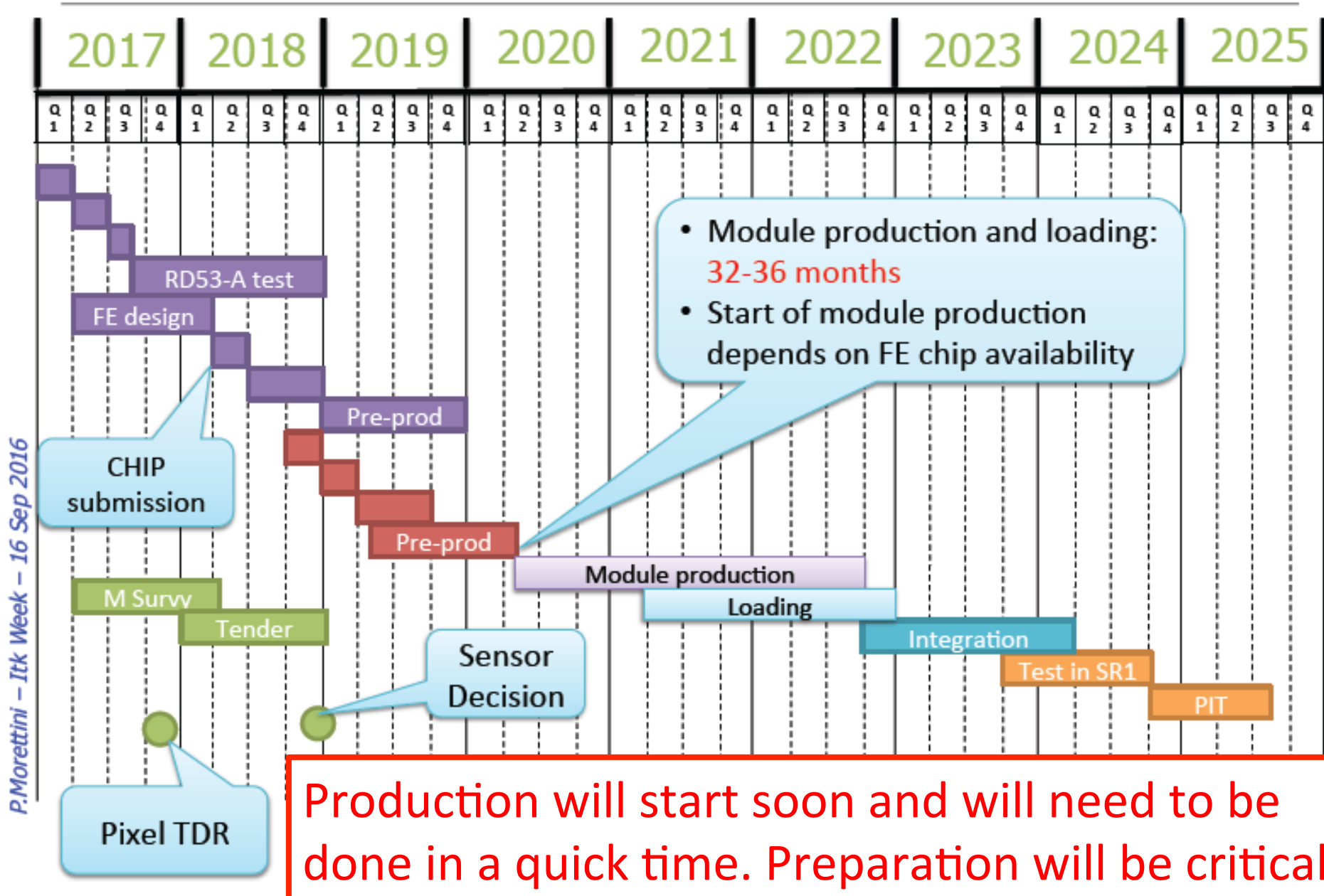
Flexes: LAPP is responsible for thermal and electrical flex design, construction and working on the flex installation procedure



Cooling: LAPP is working on the cooling infrastructure and thermal / electrical tests

Loading and cooling boxes: CPPM will have a leading role in the loading of the modules onto the staves. Material irradiation, glue qualification. This will be used as a proof of principle of the module loading infrastructure

Pixel timeline



Implication of IN2P3

Laboratoire	Nombre de physiciens (ETP)	Nombre d'IT (ETP)	CDD en mois
CPPM	6 (1.8)	6 (2.1)	60
LAL	4 (1.4)	5 (2.4)	72
LAPP	5 (2.8)	12 (6.4)	108 (+36 si production raccords CO ₂)
LPNHE	3 (1.4)	5 (2.5)	72
LPSC	4 (1.0)	10 (1.7)	144
Total	22 (8.2)	38 (15.1)	456 + 36

Significant number of physicists and ITA already involved in ITk activities

Number of FTE is expected to increase with the start of the construction. Other persons are also expected to join when the Run 2 will end (already indication for an augmentation of more than 50% of FTEs for 2018-2023)

Nevertheless a strong support is asked to the IN2P3 in terms of CDDs and lab resources to complete the task

Implication of IN2P3 (continued)

Core: contributions recognized in ATLAS (cost of deliverables)

Non-core: correlated support (laboratory infrastructure)

Sous-détecteur	Core	Non-core	CDD	Aléas	Total
Trajectographe	11.100	2.575	2.660	0.900	17.235
Calorimètres	4.160	1.260	0.630	0.340	6.280
HGTD	1.970	0.440	0.371	0.238	2.949
Fonds communs	1.485	0	0	0	1.425
Total	18.715	4.275	3.661	1.478	28.129

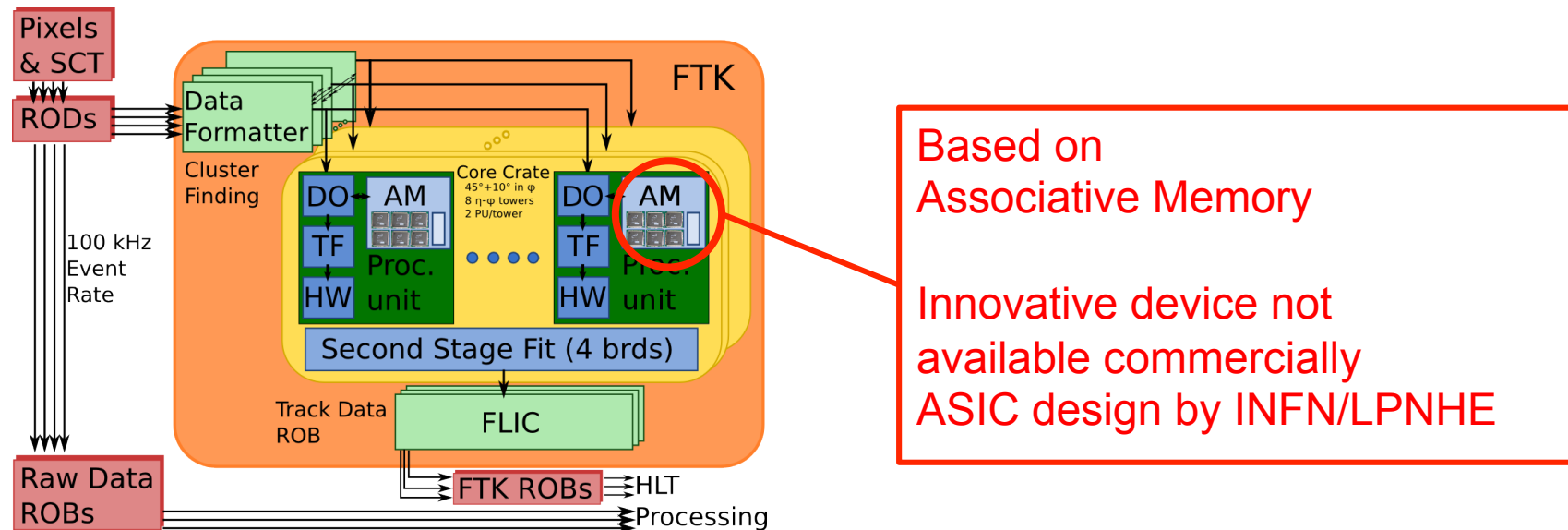
	Coût en MCHF
Déclenchement et acquisition (FTK inclus)	43.31
Trajectographe (ITk)	120.36
Calorimètre à argon liquide (HGTD inclu)	45.98
Calorimètre à tuiles scintillantes	8.58
Système de détection des muons	34.08
Détecteur à l'avant	1.30
Intégration et installation	17.42
Total	271.04

Track trigger upgrade (FTK++)

Present FTK system and FTK++ upgrade

ATLAS is installing FTK, an hardware track trigger pre-processor that will provide full detector tracking of particles with $P_t > 1$ Gev to the HLT

Installation/commissioning is ongoing now, the system will be fully operational for Phase-I



The current FTK system will not scale to HL-LHC with the current P_t threshold. The FTK++ is the proposed upgrade in the current TDAQ Phase-II scheme.

The Associative Memory is a device that finds matches between a combination of input data (silicon detector hits) and stored patterns (trajectories).

Standard memory



Too slow / not useful (information on address not needed)

Associative memory (AM)



This combinatorial pattern matching is a computational intensive operation that is performed in real-time with the AM



Amchip06 used in ATLAS FTK
(resp. LPNHE/INFN)

128 kpatterns/chip

100MHz

8*16 bit input busses

Variable Resolution (ternary bits)

High Speed Serial Link interface (2-2.4 gbps)

~8000 chips used by FTK → 1 billion patterns

FTK++

Current estimates for FTK++: 13 billion patterns

Minimum speed goal: 250 MHz (400 MHz max)

Multiple output links to increase bandwidth

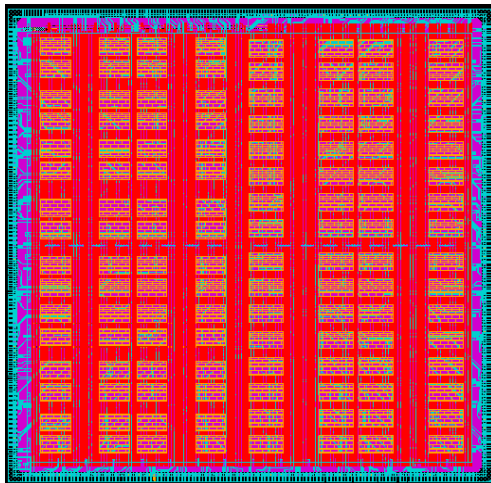
512K pattern/chip

A new chip is needed: AM09

Current prototype plan:

AM07 (2017) → AM08 (2018-2019) → AM09 (2019-2020)

(Am07 demonstrator, 28nm)



AM07B (INFN + IN2P3)

10 mm² @ TSMC 28 nm

16k patterns

200 MHz matching

AM08 same area of AM07 but final solutions

(example: 400MHz)

AM09 full-scale

(AM07 die produced, package will arrive Aug 2017)

For the time being mainly at LPNHE, (in collaboration with IPNL Lyon (CMS) in the framework of an ANR) but strategic activity (big visibility for France, with a limited effort)

Conclusions

The ITk upgrade is an important opportunity for IN2P3 laboratories in terms of technological development, visibility and responsibility.

The IN2P3 groups have covered very important roles in the ATLAS pixels and IBL construction and are presently among the leading institutions in many different sectors of the ITk

Laboratories are generally strongly oriented in supporting the activity (several recommendations by local Scientific Councils)

Given the important role and responsibilities of the groups, we ask the IN2P3 to secure an adequate support in terms of technical resources and manpower for the timescale of the operation.

Disclaimer: we are now moving to a work model in which R&D is replaced by construction plans. Anyhow the inner part of ITk has to be replaced at half of Phase-2. Some important R&D will continue (HV-CMOS, u-channels, readout electronics)